Effect of Interface States on the Performance of Antimonide nMOSFETs

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***Abstract*—Antimonide (Sb) quantum-well MOSFETs are demonstrated with an integrated high-κ dielectric (1-nm Al_2O_3/10-nm HfO_2). The effect of interface trap density D_{it} on the dc drive current and transconductance g_m is studied in detail using split C–V/G–V, pulsed I–V, and radio-frequency measurements. Pulsed I–V measurements show improved ON current, transconductance, and subthreshold slope due to reduced charge trapping in the dielectric at high frequencies. The long-channel Sb nMOSFET exhibits effective electron mobility of 6000 $cm^2/V \cdot s$ at high field ($2 \times 10^{12}/cm^2$ of charge density N_s), which is 15$\times$ higher than Si NMOS inversion layer mobility, and one of the highest values reported for III–V MOSFETs. The short-channel Sb nMOSFET ($L_G = 150$ nm) exhibits a cutoff frequency f_T of 120 GHz, an $f_T \times L_G$ product of 18 GHz $\cdot$ μm, and a source-side injection velocity v_{eff} of 2.7×10^7 cm/s at a drain bias V_{DS} of 0.75 V and a gate overdrive of 0.6 V.**

***Index Terms*—Antimonide MOSFET, high-κ dielectric, InAsSb, interface states.**

I. Introduction

An antimony-based $InAs_xSb_{1-x}$ quantum-well (QW) heterostructure with high electron mobility, integrated with high hole mobility strained $In_xGa_{1-x}Sb$ QW, can potentially enable III–V CMOS and share the same metamorphic buffer on silicon [1]. In this letter, we report $InAs_{0.8}Sb_{0.2}$ nMOSFETs with an integrated high-κ dielectric, which exhibit record-high long-channel electron mobility, short-channel electron velocity, and high-frequency small-signal performance. The effect of interface trap density D_{it}, which degrades the dc drive current and transconductance g_m, is studied in detail using split C–V/G–V, pulsed I–V, and radio-frequency (RF) measurements.

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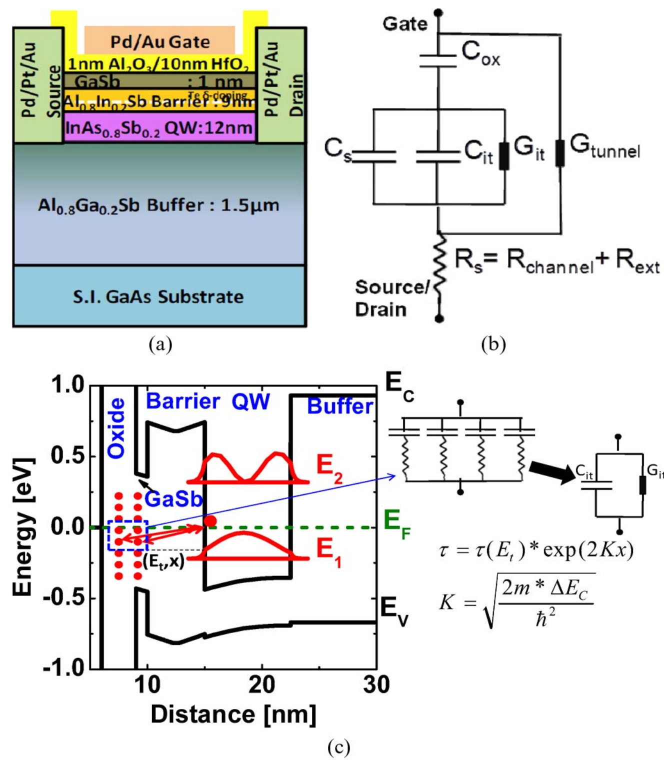

Fig. 1. (a) Schematic of the Sb nMOSFET with a 1-nm Al_2O_3/10-nm HfO_2 dielectric. (b) Equivalent-circuit model for the QW MOSFET with traps at the dielectric–GaSb interface: C_{ox} is the oxide capacitance; C_s is the semiconductor capacitance, which is the series combination of barrier and QW capacitance values; C_{it} and G_{it} are the interface trap capacitance and conductance, respectively; G_{tunnel} is the leakage conductance; and R_s is the series resistance. (c) Band diagram under the gate showing traps at the GaSb–dielectric interface exchanging carriers with the QW through tunneling. C_{it} and G_{it} are modeled using a distributed network of traps physically extending into the dielectric from the GaSb–dielectric interface.

II. Device Layer Design and Fabrication

Fig. 1(a) shows the schematic of an $InAs_{0.8}Sb_{0.2}$ nMOSFET with a 1-nm Al_2O_3/10-nm HfO_2 high-κ gate dielectric. We obtained Hall mobility of 13 500 $cm^2/V \cdot s$ at a carrier density of $2.2 \times 10^{12}/cm^2$ for the as-grown device layers without the dielectric. The devices were fabricated using a process detailed in [2], with gate lengths of 20 μm, 450 nm, 300 nm, and 150 nm.

The equivalent small-signal model for the QW MOSFET is shown in Fig. 1(b). The traps in antimonide MOSFETs not only exist at the interface but also physically extend into the dielectric (border traps) or the transition layer between the high-$kappa$ dielectric and the antimonide (defect-induced gap states, DIGS). A distributed network of traps physically extending into the dielectric from the GaSb–dielectric interface was used to model the effects of these border traps/DIGS [see Fig. 1(c)].

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14. ABSTRACT
Antimonide (Sb) quantum-well MOSFETs are demonstrated with an integrated high-κ dielectric (1-nm Al2O3/10-nm HfO2). The effect of interface trap density Dit on the dc drive current and transconductance gm is studied in detail using split C?V/G?V , pulsed I?V , and radio-frequency measurements. Pulsed I?V measurements show improved ON current, transconductance, and subthreshold slope due to reduced charge trapping in the dielectric at high frequencies. The long-channel Sb nMOSFET exhibits effective electron mobility of 6000 cm2/V ? s at high field (2 ? 1012/cm2 of charge density Ns), which is 15? higher than Si NMOS inversion layer mobility and one of the highest values reported for III?V MOSFETs. The short-channel Sb nMOSFET (LG = 150 nm) exhibits a cutoff frequency fT of 120 GHz, an fT ? LG product of 18 GHz ? μm and a source-side injection velocity veff of 2.7 ? 107 cm/s at a drain bias VDS of 0.75 V and a gate overdrive of 0.6 V.

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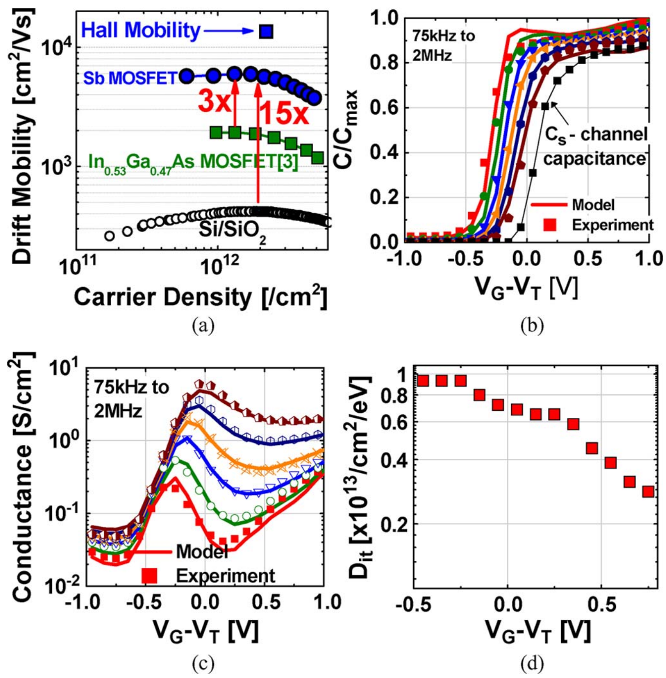

Fig. 2. (a) Extracted electron drift mobility versus N_s showing record high mobility. (b) and (c) Measured split C–V/G–V characteristics along with self-consistently modeled C–V/G–V based on the equivalent-circuit method. The value of $C_{\rm ox}$ used for the modeling is 2.3 μF/cm^2, and $C_{\max}$ is 0.8 μF/cm^2. (d) $D_{\rm it}$ extracted from self-consistent equivalent-circuit modeling of C–V/G–V.

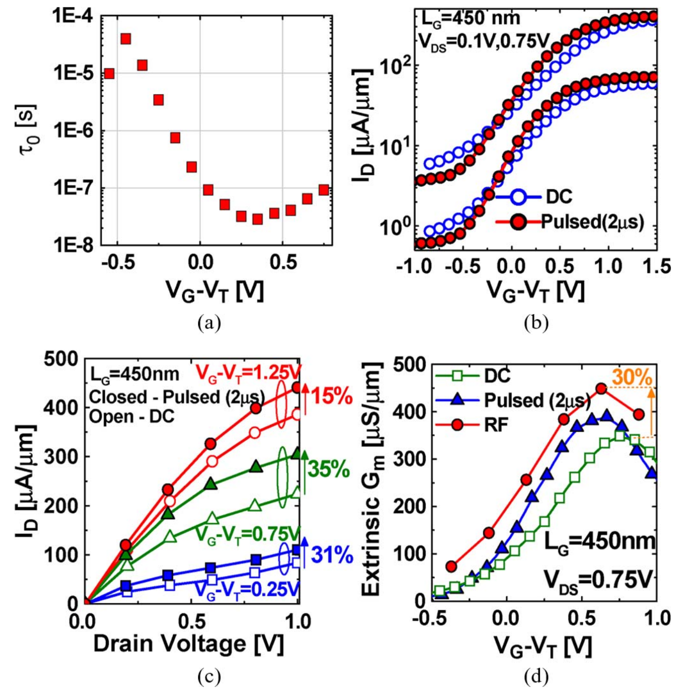

Fig. 3. (a) Response time of the traps at the GaSb/high-κ dielectric interface at $x = 0$ extracted from self-consistent equivalent-circuit modeling of C–V/G–V. (b) Pulsed I_D–V_G measurements showing improved $I_{\rm ON}$ and subthreshold slope compared with dc. (c) Pulsed I_D–V_D characteristics showing significant enhancement in $I_{\rm ON}$ over dc. (d) Extrinsic RF g_m showing 30% enhancement over dc g_m due to less charge trapping in RF.

III. Equivalent-Circuit Modeling and Interface State Characterization

The equivalent-circuit modeling technique relies on self-consistently solving the capacitance and conductance contributions from interface states, without needing information about the location of conductance peaks. The fitting procedure minimizes the error between the measured admittance (C–V and G–V) and the simulated admittance for the device over the entire frequency range while solving for $D_{\rm it}$, the trap time constant, and the semiconductor capacitance. The procedure is explained in detail in our earlier publication [4]. Traps extending until 1 nm deep into the oxide/transition layer have been considered for the C–V/G–V model, with the trap profile exponentially decaying into the oxide as given by $N_{\rm it}(x) = N_{\rm it}(0)\exp(-x/x_{\rm DIGS})$ [5]. The characteristic decay length $x_{\rm DIGS}$ was used as a fitting parameter and was defined to be 1 Å for this modeling. As traps extend into the oxide, their response time exponentially increases as $\tau = \tau_0(E_t)\exp(2kx)$, where $\tau_0(E_t)$ is the response time of traps at $x = 0$ at a given energy level E_t [6]. The wave vector for the electrons tunneling from the conduction band in the InAsSb QW to the traps at the GaSb/high-κ dielectric interface ($k = \sqrt{2m * \Delta Ec/\hbar^2}$) is estimated to be ~ 0.13/Å using $\Delta Ec = 1.3$ eV [5], [6]. The effect of these traps on the electron mobility is studied next using detailed split C–V/G–V modeling.

Fig. 2(a) shows the electron drift mobility extracted from the output conductance and measured C–V characteristics. We report a record-high effective electron mobility value of 6000 $\mathrm{cm^2/V \cdot s}$ at $2 \times 10^{12}/\mathrm{cm}^2$ of N_s, which is 15× higher than Si NMOS inversion layer mobility and 3× higher than that of InGaAs NMOS [3]. The extracted drift mobility is lower than the Hall mobility partly due to the overestimation of charge from split C–V measurements due to the effect of interface states $D_{\rm it}$. Fig. 2(b) and (c) shows the measured split C–V/G–V characteristics of the $L_G = 20$ μm device. The frequency dispersion in the C–V/G–V characteristics is due to $D_{\rm it}$. The measured C–V and G–V data are modeled using the equivalent-circuit method in [4] based on the model in Fig. 1(b), including the effects of border traps [5]–[7]. The measured and modeled C–V/G–V curves are in excellent agreement with each other, as shown in Fig. 2(b) and (c). Fig. 2(d) shows the extracted $D_{\rm it}$ from the equivalent-circuit modeling. The $D_{\rm it}$ shown in Fig. 2(d) is the net integral of traps at the GaSb/high-κ dielectric interface (interface traps) and those extending into the oxide (border traps) at a given energy level. Charging and discharging of interface traps give rise to stretch out in the measured split C–V. Hence, the inversion charge obtained from the measured C–V is overestimated, resulting in a lower value for drift mobility obtained using output conductance $g_{\rm DS}$ and N_s from split C–V.

Fig. 3(a) shows the trap time constant extracted from the C–V/G–V modeling. The time constant shown in Fig. 3(a) is the response time of the traps at the GaSb/high-κ dielectric interface at $x = 0$ (τ_0). At each gate bias, the time constant of the traps would follow $\tau = \tau_0(E_t)\exp(2kx)$, and the trap density follows $N_{it}(x) = N_{it}(0)\exp(-x/x_{\rm DIGS})$, depending on the depth x. The net trap response would then be driven by the physical depth of the traps into the oxide, $\tau(x)$, and $N_{it}(x)$. To demonstrate the impact of traps on the device performance, pulsed I–V measurements (2-μs pulsewidth) and RF measurements were performed. Pulsed measurements show a significant improvement (by 35% at a 0.75-V gate overdrive)

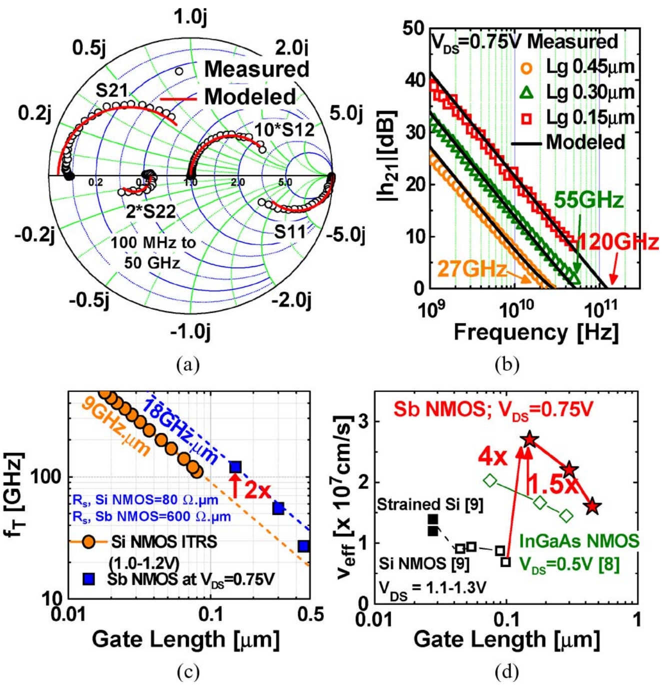

Fig. 4. (a) Measured and modeled S-parameters of the 150-nm L_G Sb NMOS at $V_G - V_T = 0.6$ V and $V_{\mathrm{DS}} = 0.75$ V. (b) Measured and modeled $|h_{21}|$. (c) f_T versus L_G. (d) Extracted source injection velocity.

in I_{ON} and subthreshold slope [see Fig. 3(b) and (c)] of these devices compared with the dc measurements. The 35% gain in the ON-state current measured at a high overdrive indicates that majority of the traps contributing to drive degradation exist deeply within the oxide and have time constants $> 2\ \mu$s. Fig. 3(d) shows extrinsic g_m comparing dc, pulsed I–V, and RF measurements. Peak extrinsic RF g_m improves by 30% compared with dc g_m for a gate overdrive of 0.6 V. This improvement is due to reduced charge trapping in the dielectric at very high frequencies. This confirms that the reduction in FET mobility compared with Hall mobility is partly due to the overestimation of charge from split C–V, and the actual electron mobility in the Sb MOSFET should be higher than the measured dc value of 6000 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$.

IV. RF Characterization

Fig. 4(a) shows the measured and modeled scattering parameters (S-parameters) of the 150-nm L_G device from 100 MHz to 50 GHz. An excellent agreement between the measured and simulated S-parameters confirms the extracted circuit element values. Fig. 4(b) shows the measured and modeled small-signal current gain $|h_{21}|$ versus frequency for $L_G = 150$, 300, and 450 nm. The devices have cutoff frequencies of 120, 55, and 27 GHz, respectively. From the extracted parameters from small-signal modeling, we evaluate the source-side injection velocity v_{eff} of these devices as g_m/slope (C_{gs} versus L_G). Fig. 4(c) and (d) benchmarks the f_T and v_{eff} of the Sb NMOS devices with state-of-the-art Si and III–V NMOS. The 150-nm L_G Sb NMOS exhibits a v_{eff} of 2.7×10^7 cm/s and an $f_T \times L_G$ product of 18 GHz $\cdot\ \mu$m. The measured f_T and $f_T \times L_G$ are 2× higher, and v_{eff} is 4× higher than Si NMOS (1.0–1.2 V V_{DD}) at similar L_G.

V. Conclusion

Long-channel Sb NMOS devices are demonstrated with high field effective electron mobility of 6000 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$. Short-channel Sb NMOS devices exhibit a cutoff frequency f_T of 120 GHz, an $f_T \times L_G$ product of 18 GHz $\cdot\ \mu$m, and a source-side injection velocity v_{eff} of 2.7×10^7 cm/s at 0.75-V V_{DS} and 0.6-V gate overdrive. The measured f_T and $f_T \times L_G$ are 2× higher, whereas v_{eff} is 4× higher than Si NMOS (1.0–1.2 V V_{DD}). The 150-nm L_G device exhibits a drive current of 450 μA/μm at V_{DS} of 0.75 V. Charging and discharging of D_{it} give rise to stretch out in the measured split C–V curves, resulting in a lower value for extracted drift mobility. Pulsed I–V and RF measurements show enhanced I_{ON}, subthreshold slope, and g_m compared with dc measurements due to reduced trap charging effects at high frequencies.

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